IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
MARK A. GAJDA
Serial No.
Filed: CONCURRENTLY
TRENCH-GATE SEMICONDUCTOR DEVICES, AND THEIR MANUFACTURE

Atty. Docket
GB010121A

Commissioner for Patents
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Before line 1, insert the following new paragraph:

--This is a Divisional of Application Serial No. 10/197,651, filed July 17, 2002.--

IN THE CLAIMS

Claims 1-6 (canceled).

7. (Original) A method of manufacturing a trench-gate semiconductor device having source and drain regions which are separated by a channel-accommodating region adjacent to the trench-gate, including the following sequence of steps:

(a) providing at a surface of a semiconductor body a masking pattern having therein a window that is used for self-aligning a gate trench and parts of the gate formed in the subsequent steps (b) to (d);

(b) etching the trench into the semiconductor body within the window, and forming a dielectric layer at the walls of the